REMARKS

Claims 1, 7, 9 to 12, 15, 17 to 19, 21, 22, 25, 27, 91, 96 to 99, 101 to 103, 108 to 114 and 116 to 139 are pending for examination in the present application, with Claims 1, 9, 15 and 129 being the pending independent claims. Claims 9, 15, 118, 129 and 133 are amended herein. Claims 4, 29, 30 and 115 were previously withdrawn. No new claims are added, and no claims are newly canceled herein. No new matter is believed to be added herein. Entry hereof and early passage to issue are respectfully requested.

Claim Rejections – 35 USC § 103

Claims 1, 7, 9-12, 15, 17-19, 21, 22, 25, 27, 91, 96-99, 101-103, 108-114 and 116-139 are rejected under 35 USC § 103(a) over Lin (U.S. Pat. No. 6,303,423) in view of Nakanishi (U.S. Pat. No. 6,921,980). Reconsideration and withdrawal of these rejections are respectfully requested.

Claim 1

Claim 1 is directed to an integrated circuit chip. The chip includes a semiconductor substrate and a transistor in and on said semiconductor substrate. Multiple metal and dielectric layers are over said semiconductor substrate. A first contact pad is over said semiconductor substrate. A second contact pad is over said semiconductor substrate. A passivation layer is over said multiple metal and dielectric layers, wherein said passivation layer comprises a nitride. A first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening. A second opening in said passivation layer is over a second contact point of said second contact pad, and said second contact point is at a bottom of said second opening. A power metal structure is over said passivation layer and on said first contact point. The power metal structure is connected to said first contact point through said first opening. The power metal structure comprises a copper layer. The power metal structure has a first region configured to be wirebonded thereto for connection made to a next level of packaging. A ground metal structure is over said passivation layer and on said second contact point. The ground metal structure is connected to said second contact point through said second opening. The ground metal structure comprises a copper layer. The ground metal structure has a second region configured to be wirebonded thereto for connection made to said

next level of packaging. A capacitor is over said passivation layer, vertically over said power and ground metal structures and vertically over said first contact point. A first solder joint is vertically over said first contact point and between a first terminal of said capacitor and said power metal structure, wherein said first solder joint connects said first terminal to said power metal structure. A second solder joint is between a second terminal of said capacitor and said ground metal structure, wherein said second solder joint connects said second terminal to said ground metal structure.

Claim 15

Claim 15 is directed to an integrated circuit chip comprising a semiconductor substrate and a transistor in and on said semiconductor substrate. Multiple metal and dielectric layers are over said semiconductor substrate. A first contact pad is over said semiconductor substrate. A passivation layer is over said multiple metal and dielectric layers, wherein said passivation layer comprises a nitride, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening. A second contact pad is over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening. A third contact pad over said semiconductor substrate, wherein said third contact pad is connected to said first contact point through said first opening and connected to said second contact pad, wherein said third contact pad has a region that is configured to be wirebonded thereto for connection made to a next level of packaging and is horizontally offset from said first contact point. A first polymer layer over said passivation layer, wherein a second opening in said first polymer layer is over a second contact point of said second contact pad, and said second contact point is at a bottom of said second opening. A capacitor over said first polymer layer and said second contact point. A solder joint is between said second contact point and a terminal of said capacitor, wherein said solder joint connects said terminal to said second contact point.

The applied references, either alone or in combination, are not seen to disclose or suggest the foregoing combination of features of each of independent Claims 1 and 15.

In this regard, The Examiner asserts in the Office Action that "vertically over simply suggest above" and that "it does not appear that applicant's capacitor electrodes are all directly

over the said first point (see for example right electrode 23 of Figure 3 which is not directly over 16)". See Office Action, p. 21, lines 10-15. Applicants respectfully disagree.

The wording of "vertically over" means overlying in a substantially vertical direction. Accordingly, the claimed subject matter of a capacitor 38 over said passivation layer 18, vertically over said power and ground metal structures (left and right portions 23) and vertically over said first contact point (left contact point 16 at a bottom of a left opening in the passivation layer 18) is believed to be supported in Fig. 3 and related description in the specification.

The Examiner further contends that "[i]t is also noted that just because a part of an integrated circuit (such as capacitor 54 of Lin's Figure 10) is shown connected to an internal pad of a die (such as pad 16 of Figure 10 of Lin), it does not exclude the possibility of making other connections (including connections to external components) to the capacitor 54. How various components are interconnected depends on circuit design and the present claims do not recite any specific circuit details that would specifically not allow multiple connections to a component (such as interconnection with both an internal and external component), and neither has applicant provided any evidence in support of the above." See Office Action, pg. 22, lines 2-10.

In response to the Examiner's contention, Nakanishi provides a circuit design with a wiring trace 5 for both internal and external connections to a discrete electronic component 48. See Nakanishi, Figs. 2(a)-2(e), 3(a) and 3(b). Nevertheless, Lin's capacitor 54 is not disclosed to be connected to an external circuit, and Lin is not seen to consider or address a connection between Lin's capacitor 54 and an external circuit. Accordingly, even if Lin's capacitor 54 were to be configured for internal and external connections, like Nakanishi's device, Nakanishi's circuit design would be applied to Lin's device, such that the design of the arrangement of a capacitor, a wiring trace and an electrode pad would follow that of Nakanishi's discrete electronic component 48, Nakanishi's wiring trace 5 and Nakanishi's electrode pad 3. Thereby, the electrode pad would be set in a peripherial area, as shown in Fig. 1a of Nakanishi, but would not be set in a center region and under the capacitor because Nakanishi fails to teach, hint or suggest an advantage or motivation of setting a shortest path between Nakanishi's capacitor 8 and the IC metal of a chip, which makes Nakanishi's capacitor 8 able to provide power for the activated active circuit faster than the power is provided through Nakanishi's wiring trace 25 to the activated active circuit. In the regard, the claimed subject matter of "a capacitor .....

vertically over said first contact point" is not believed to be obvious in view of Lin's teaching and Nakanishi's teaching.

Also, the Examiner contends that the claimed first contact pad can be alledged to be a contact pad in Nakanishi nearest to 8 to which 8 is connected. See Office Action, p. 16, lines 9 and 10. Applicants respectfully disagree because the alledged first contact pad in Nakanishi has no first contact point at a bottom of a first opening in Nakanishi's lower insulating film 4, which is assumed to be alleged by the Examiner to be the claimed passivation layer based on lines 12 and 13 on p. 16 of the Office Action. Accordingly, Nakanishi's contact pad nearest to 8 to which 8 is connected is not believed to be the same as the claimed first contact pad.

In view of the above, the applied references are not seen to disclose or suggest the claimed features of "a capacitor is over said passivation layer, vertically over said power and ground metal structures and vertically over said first contact point" and "a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening" as claimed in Claim 1. Similarly, the applied references are not seen to disclose or suggest the claimed features of "a capacitor is over said first polymer layer and said second contact point" and "a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening" as claimed in Claim 15.

Accordingly, Claims 1 and 15 are believed to be allowable over the applied references. Reconsideration and withdrawal of the rejections of Claims 1 and 15 are respectfully requested.

Claim 9

Claim 9 is directed to an integrated circuit chip comprising a semiconductor substrate and a transistor in and on said semiconductor substrate. Multiple metal and dielectric layers are over said semiconductor substrate. A first contact pad is over said semiconductor substrate. A passivation layer is over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening, wherein said passivation layer comprises a nitride. A second contact pad is over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening, wherein said second contact pad comprises a first substantive gold layer with a thickness greater than 1 micrometer. A capacitor is over said

passivation layer and said second contact pad. A solder joint is between a terminal of said capacitor and said second contact pad, wherein said solder joint connects said terminal to said second contact pad. A third contact pad between said solder joint and said second contact pad, wherein said third contact pad comprises electroplated copper, wherein a contact area between said third contact pad and said second contact pad is horizontally offset from said first contact point.

Claim 129

Claim 129 is directed to an integrated circuit chip comprising a semiconductor substrate and a transistor in and on said semiconductor substrate. Multiple metal and dielectric layers are over said semiconductor substrate. A first contact pad is over said semiconductor substrate. A passivation layer is over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening, wherein said passivation layer comprises a nitride. A second contact pad is over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening, wherein said second contact pad comprises a first gold layer with a thickness greater than 1 micrometer. A capacitor is over said passivation layer and over said second contact pad. A solder joint between a terminal of said capacitor and said second contact pad, wherein said solder joint connects said terminal to said second contact pad. A third contact pad is between said solder joint and said second contact pad, wherein said third contact pad is finished with a solder wettable material comprising gold, wherein a contact area between said third contact pad and said second contact pad is horizontally offset from said first contact point.

The applied references, either alone or in combination, are not seen to disclose or suggest the foregoing combination of features of each of independent Claims 9 and 129.

For similar reasons as those discussed above with respect to Claims 1 and 15, the applied references are not seen to disclose or suggest the claimed features of "a capacitor over said passivation layer and said second contact pad" and "a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening" as claimed in Claim 9. Similarly, the applied references are not seen to disclose or suggest the claimed features of "a capacitor

over said passivation layer and said second contact pad" and "a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening" as claimed in Claim 129.

Further, the Examiner contends that "Applicant's claims only recite gold and hence Shirasaki is pertinent, whether or not other metals are present (as these are not excluded in the recited claims)." See Office Action, p. 22, lines 13-15. This contention is believed to be rendered moot by the currently amended wording in Claims 9 and 129 to recite "a substantive gold layer" which is believed to avoid the concern of not excluding other metals.

The Examiner asserts that "it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Arvin is also in the field of semiconductor electronic devices." See Office Action, p. 23, lines 2-6.

In response to the Examiner opinion, even though Arvin's teaching is in the field of semiconductor electronic devices, Arvin's gold layer 14 has different functions than the first gold layer which is recited in Claim 9 of the present application. Arvin's gold layer 14 is taught to produce a solder wettable and socketable surface and to be finished by being bonded with Arvin's solder ball 17. See Arvin, Figs. 1 and 2A, and par. [0037]. However, the first gold layer of a second contact pad, as recited in Claim 9, allows a third contact pad to be provided between the solder joint and the second contact pad, and is not finished by being bonded with a solder joint, which has different functions from Arvin's gold layer 14. Accordingly, even if, for argument's sake, Arvin's gold layer 14 was applied to Lin's device, a contact pad would not to be considered to be provided between Arvin's gold layer 14 and Lin's contact balls 52 formed using selective solder deposition because Arvin fails to teach, hint or suggest that there could further be a contact pad comprising electroplated copper, for example, provided between Arvin's gold layer 14 and Arvin's solder ball 17. In this regard, the subject matter that a third contact pad comprising electroplated copper between said solder joint and said second contact pad comprising "a first substantive gold layer with a thickness greater than 1 micrometer," as

currently claimed in Claim 9, is believed not to be obvious over Lin's teaching in view of Arvin's teaching.

Similarly, the applied references are not seen to disclose or suggest "a first substantive gold layer with a thickness greater than 1 micrometer," as currently claimed in Claim 129.

Accordingly, Claims 9 and 129 are believed to be allowable over the applied references. Reconsideration and withdrawal of the rejections of Claims 9 and 129 are respectfully requested.

The other claims currently under consideration in the application are dependent from their respective independent claims discussed above and therefore are believed to be allowable over the applied references for at least similar reasons. Because each dependent claim is deemed to define an additional aspect of the invention, the individual consideration of each on its own merits is respectfully requested.

The absence of a reply to a specific rejection, issue, or comment does not signify agreement with or concession of that rejection, issue, or comment. In addition, because the arguments made above may not be exhaustive, there may be other reasons for patentability of any or all claims that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment or cancellation of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment or cancellation.

CONCLUSION

In view of the Amendments and Remarks herein, Applicant submits that the claims are in condition for allowance and respectfully request a notice to this effect.

Should the Examiner have any questions, the Examiner is invited to call the undersigned. All correspondence should be directed to our address given below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,

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